

PRODUCT BRIEF

## **JT1001**

Level One's NetCelerator<sup>TM</sup> network accelerator chips integrate network interface functions with protocol level processing. The JT1001 is targeted for server and workstation applications. It is the first Ethernet network accelerator to offer 10/100/1000Mbps IEEE 802.3 operation and integrated TCP/IP and VLAN processing functions in a processor-less design.

### **GENERAL DESCRIPTION**

Like all NetCelerator chips, JT1001's highly optimized architecture implements host offloading, bus acceleration, and high-speed data transfer engines in a single chip. These features increase functionality, reduce OEMs' time to market, and lower the overall cost of the network interface. Features include 10/100/1000Mbps Ethernet operation, large buffers, and optimized data transfer methods.



NetCelerator Architecture Block Diagram

# FEATURE DESCRIPTION

#### 10/100/1000Mbps Ethernet Implementation for a Cost Effective Migration Path

- Full and half-duplex operation
  - Packet Burst in half-duplex; Symmetric/asymmetric full-duplex flow control
- Physical Layer Device (PHY) Interface
  - Gigabit Media Independent Interface (GMII) for 1000BASE-T
  - Media Independent Interface (MII) for 10/100BASE
  - Ten-Bit Interface (TBI) for 1000BASE-X fiber
- 96KB embedded FIFO
  - 32KB transmit (TX), 64KB receive (RX)
  - Eliminates need for external FIFO

# Host Offloading via Chip-Level Internet

## $\label{eq:protocol} \textbf{(CLIP^{\textsc{tm}}) and Policy-Based Behavior}$

- IPv4 checksum calculation on chip
  - IP, TCP and UDP checksums supported
  - Packet filtering based on checksum errors
- 802.3ac and VLAN tag support
  - Programmable 16 entry table; Filtering based on recognized VLANs; VLAN tag stripping on receive; Global and/or per packet VLAN tag insertion on transmit

#### **Optimized Bus Transfer Operation**

- High-Speed PCI Interface
  - PCI 2.1 compliant
    - Efficient PCI master operation
    - 33MHz, 32/64 bit operation
    - 64 bit addressing
    - Supports dual address cycles
- Supports three I/O methods
  - Programmed I/O
  - Traditional scatter-gather "bus master" DMA
  - Propulsion<sup>™</sup> technology packet bursting across PCI bus increases the throughput for small packets
- Propulsion features
  - Packet bursting across PCI bus
  - Minimizes bus arbitrations
  - Eliminates logical to physical address translation
  - Scales to wider bus widths and faster clock rates
  - Minimizes interrupts by coalescing transfers across the PCI bus

#### **Additional Performance Features**

- Independent TX and RX engines
- Intelligent interrupt management
  - No interrupt on TX
  - Scheduled interrupts for data streaming
  - Programmable high/low watermark interrupts for RX and TX FIFOs

#### **Robust Drivers and Management**

- · Supporting software includes certified device drivers and end user diagnostics
  - Windows® NT 3.51, 4.0 and 5.0; Windows® 95 OSR2; Windows <sup>®</sup> 98; NetWare<sup>™</sup> 4.11 and 5.0
  - Support for the OnNow Initiative and PCI Power Management
    - Wake-on-LAN<sup>™</sup>, Magic Packet <sup>™</sup>
    - PCI PME Signal
  - Required elements of the 802.3 MIB

#### **Additional NetCelerator Features**

- EEPROM Interface
  - Single word read/writes or reads entire contents
  - Checksum after read, auto-detection
- Expansion ROM Interface
  - Supports ROM, EPROM, and flash memory
  - Internally supports up to 4K expansion ROM
  - Up to one megabyte can be supported using external logic
- · Supports up to four individually programmable LEDs
- IEEE 1149.1a-1993 (JTAG) standard compliant boundary scan

#### **Technology Features**

- State machine design
- .35 micron process •
- Plastic ball grid array (PBGA) package
- 3.3 volt/5 volt tolerant I/Os
- Targeted power consumption of less than 1.5W (typical)

#### **Product Availability**

- · Samples available now
- Production volume available 4098

#### **About Level One**

Level One Communications (Nasdaq: LEVL) provides silicon connectivity, LAN switching and WAN access solutions for high-speed telecom and networking applications. Level One combines its strengths in analog and digital circuit design, with its communications systems expertise, to produce digital and mixed-signal solutions with increased functionality and greater reliability, resulting in lower total systems cost.



- 1000Mbps SERDES
- Fiber Optic TX/RX
- 125MHz Clock

- Board
- Bracket
- Serial EEPROM

For additional information call (512) 407-2100 or visit Level One's website at www.level1.com Fax (512) 452-5592 Company headquarters are located at 9750 Goethe Road, Sacramento, CA 95827

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