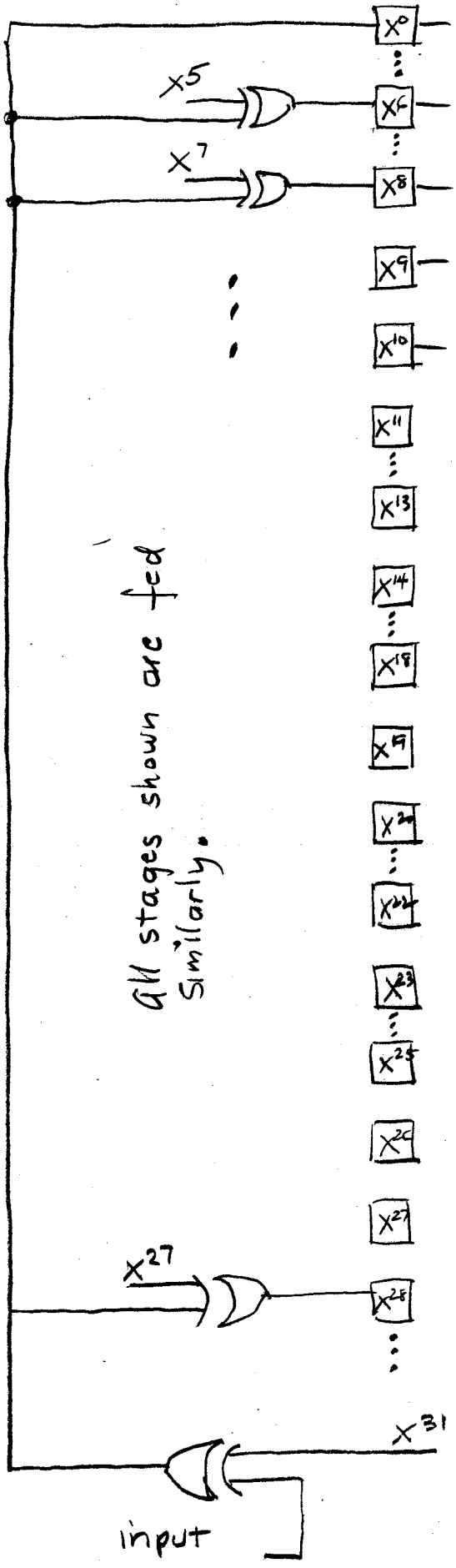
# Serial implementation of iSCSI poly G(x)




1. All stages are D-flops
2. All stages not shown are fed directly (no XOR) from preceeding stage.
3. This circuit multiplies the input poly by $x^{32}$ and divides by G(x)
4. When the last bit of the dividend has been processed the register stages contain the remainder of the division

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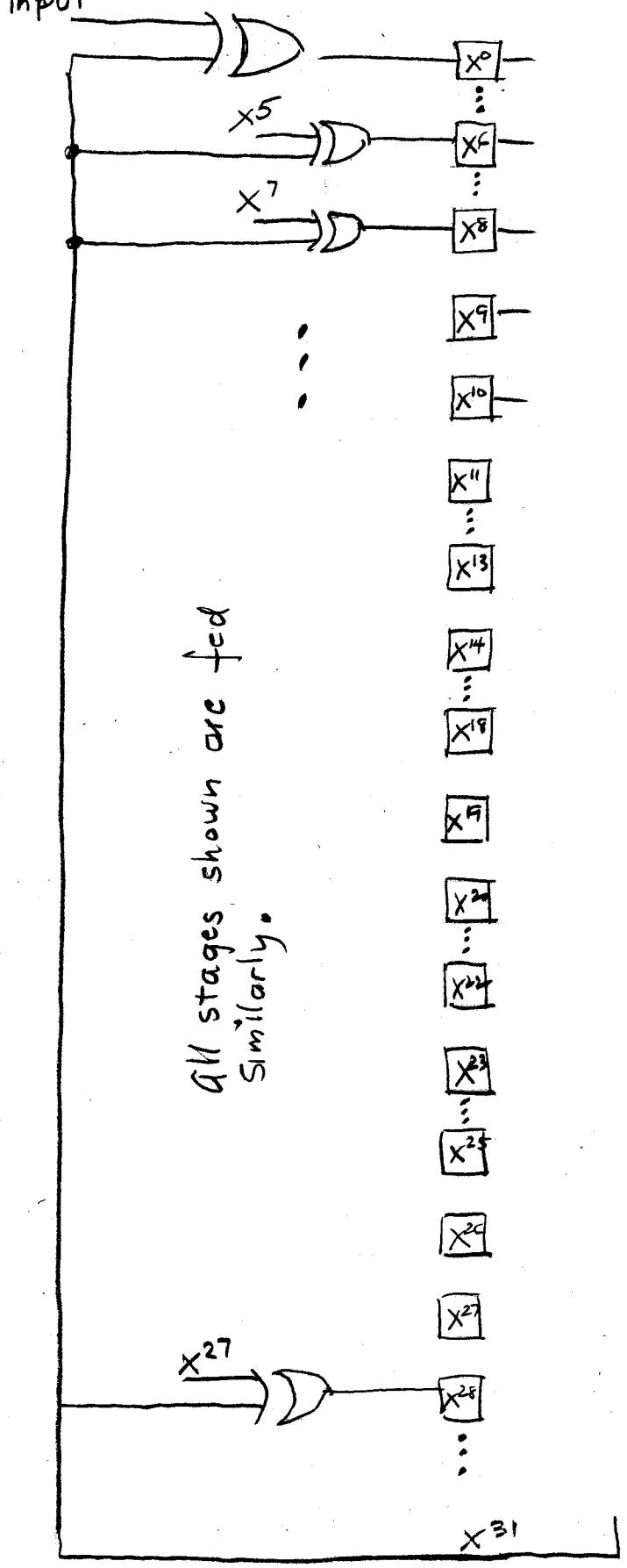


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